ISSCC 2008 Call for Papers

IEEE International Solid-State Circuits Conference

Sunday – Thursday, February 3 - 7, 2008
San Francisco Marriott Hotel, San Francisco, CA

Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG --- Op-amps and instrumentation amps, baseband amplifiers, comparators, multipliers, voltage references, power-control circuits, regulators & dc-dc converters; continuous-time & discrete-time filters; consumer electronics, non-linear analog circuits, switched-capacitor circuits; synthesizers, PLLs.

DATA CONVERTERS -- Nyquist-rate and oversampling A/D and D/A converters; sample-and-hold circuits.

HIGH-PERFORAMNCE DIGITAL --- Microprocessors; network processors; high-speed digital circuits; intra-chip communication circuits; soft error, variation and fault tolerant circuits; reconfigurable logic arrays; security circuits; clock generation and distribution circuits and architectures; high-performance logic micro-architectures and circuit techniques; implementation methodologies for high performance digital VLSI.

IMAGERS, MEMS, MEDICAL & DISPLAY --- Image sensors and companion chips; smart sensors; MEMS for analog and RF; MEMS for sensor-and-instrumentation applications, integrated sensors and transducers; sensor-interface circuits; biosensors; microarrays and lab-on-a-chip; sensors for medical applications; circuitry and MEMS technologies that enable bio-medical and environmental applications; display drivers, controllers, and companion chips; thin-film-transistor interface circuits; organic LED and liquid-crystal-display interface circuits; flat-panel and projection displays; circuits for print heads.

LOW-POWER DIGITAL --- Cell phone processor and baseband architectures; graphics processors; digital-noise isolation techniques; low-power logic micro-architectures and circuit techniques; energy recovery techniques, energy-adaptive circuit techniques, adaptive body bias circuits; power reduction and management methods for digital VLSI, on-chip PVT sensing circuits; adaptive voltage and frequency scaling; multi-length transistor design methodologies; power estimation methodologies.

MEMORY --- Static, dynamic, non-volatile, and read-only memory; circuit-design techniques, system architectures, I/O interfaces, and array organizations; magnetic and ferro-electric memory designs and architectures; data storage and multi-bit-cell-based memory designs; embedded memory architectures, cache-memory systems, multi-port memory, and CAM designs; emerging memory technologies: nano-crystal, phase-change, and 3D memories; high-speed low-power and low-voltage memory designs; yield-enhancement redundancy, and ECC techniques; memory testing and built-in self-test.

RF --- Circuits and sub-circuits for RF/IF/baseband, including receiver and transmitter front-end circuits, narrowband RF, ultrawideband and millimeter-wave circuits (MMDS, 60GHz), IF amplifiers, power amplifiers, RF switches, power detectors, active antennas - including MIMO, modulators, demodulators.

TECHNOLOGY DIRECTIONS --- Advanced circuit technologies and techniques; ultra-low-voltage and sub-threshold logic design; molecular-, organic-, and nano-electronics; flexible substrates and printable electronics; 3D-integration and novel packaging technologies; compound-semiconductor, superconductive, and micro-photonic technologies and circuits; energy sources and energy harvesting; emerging applications such as bio-medical and ambient-intelligence; emerging wireless applications and circuits; 3D RF and mixed-signal circuits; RFID; advanced signal-processing and microprocessor architectures; design for manufacturability; analog and optical processors, non-transistor-based analog and digital circuits and their system architectures; advanced memory technologies; spintronics; quantum storage.

WIRELESS --- Receivers, transmitters, and transceivers for wireless systems including (but not limited to) WLAN, WPAN, WMAN, GPS, DVB/DMB, Bluetooth, UWB, GSM/EDGE/CDMA/UMTS/3G/4G base stations and handsets, TV, radio, satellite, and ISM band systems.

WIRELINE --- Receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, cable-modem; optical/electrical data links and backplane transceivers, power-line/phone-line home networks, subscriber-line circuits and modems. Wireline transceiver building blocks like AGC, oscillators, line-drivers and hybrids.

A submission may be accepted as either a regular paper or a short paper. A regular paper is allowed 23 minutes for presentation and 7 minutes for questions. Short papers are allowed 15 minutes total for both presentation and questions. Regular and short papers have the same submission requirements and quality standards. They differ only in the determination by the Program Committee of the time required to present their key ideas. Companion papers for large chips, ones that require two paper slots to discuss both architecture and circuit details, are encouraged (identify companion papers during the submission). Please refer to the sample Abstract on the ISSCC Web site (www.isscc.org/isscc).

• 2008 Conference Theme •
"System Integration for Life and Style"

Submission Deadline is Monday, September 17, 2007
3:00PM Eastern Standard Time (19:00 GMT)